A Highly Integrated, Versatile GPS Receiver for E911 Applications

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Abstract — **This paper presents the design of a highly integrated GPS receiver for hand held and other applications. The IC consists of a complete GPS receiver with an integrated multi-mode fractional-N synthesizer. It is one of the most highly integrated GPS receiver ICs presented to date with unmatched flexibility and performance. The receiver chip is fabricated in a 0.35μm silicon BiCMOS process and packaged in a 48 pin 7mm x7mm land grid array chip scale package.**

I. INTRODUCTION

The US government began using GPS as a navigational aid in 1980. The first hand held commercial GPS products were introduced in 1991. Since then, GPS use has steadily increased for commercial navigation and positioning. One emerging application for GPS is next generation cell phones that must incorporate positioning technology to comply with the FCC's enhanced 911 regulations.

The STORM RFIC is a single chip GPS receiver, which builds upon previous generation CONEXANT ICs [1]. This next generation GPS receiver uses a low IF architecture to reduce cost and minimize potential interference from co-located transceivers within a hand held device. This IC consists of an integrated LNA, I/Q down converter, VCO, crystal buffer/oscillator, multi-mode ΔΣ fractional-N PLL, IF filter, IF AGC, multi-mode quantizer and dual slope A/D with temperature sensor. A recent GPS paper reports high integration but requires an external TCXO and IF filter for cell phone applications [2]. It also does not have the versatility of this design. This paper will describe the architecture and flexibility of the GPS receiver as well as key portions of the design enabling the high level of integration.

II. REQUIREMENTS

The target application for this design is next generation cell phones that require positioning information for emergency situations. As with all hand held applications, cost, power and size are of major concern. Time to market was also a major concern, which necessitated the reuse of current and previous CONEXANT circuit designs. The design required that the single IC receive the GPS L1 (1575.42MHz, 154Fo, where Fo=10.23MHz, the P code chipping rate) satellite signal at -130dBm minimum. The RFIC must provide a digitized output with 1.5 or 2 bits of resolution for input to a DSP at CMOS levels. Since cell phones already have a stable oscillator, the PLL reference input was required to accept any signal from 5 MHz to 30MHz or generate its own reference over that same range with the proper external crystal. The IC also buffers the reference clock to the baseband IC at either CMOS or differential LVDS levels.

An on chip temperature sensor was included along with a dual slope A/D so that the controller chip can compensate for frequency drift of a low cost crystal. This A/D also has four external inputs that can measure external signals. One application is to measure the wheel tick information generated from a gyro for dead reckoning navigation.

III. ARCHITECTURE AND DESIGN

Most GPS receivers use a dual conversion architecture that requires an external IF filter. Figure 5 shows a block diagram of the STORM receiver. A low IF architecture was implemented to reduce external parts count which lowers system cost and size. It also improves the out of band interference rejection since the IF filter is moved forward in the gain plan. A low IF system allows the use of capacitive coupling in the IF which reduces the dc offset and 1/f noise problems associated with zero IF systems. For stand alone systems, an external crystal at 10.949MHz and 21.898MHz can be used with the integer dividers to reduce power consumption by shutting off the fractional synthesizer. Since most cell phones have a stable source that is not at either of these frequencies, a fractional N synthesizer with ΔΣ modulation is included to eliminate the need for a special crystal.

An internal LNA is included to improve sensitivity and allow the use of a post selector filter to improve out of band rejection. The internal LNA can be bypassed when the receiver is used with an external antenna that has a built-in LNA. At the mixer input the signal is converted to a differential signal to reduce noise and substrate coupling. The down converter creates I and Q signals at the low IF which are then filtered with linear phase filters. The IF filters have the ability to switch between wide and narrow bandwidth to allow for baseband multipath resolution techniques. The IF AGC is completely

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controlled internal to the chip and is set to achieve a probability of 40 percent 1's at the digital outputs.

Each section of the chip can be powered up and down independently and is controlled through a three-wire bus, which provides the interface to the GPS baseband chip or an external controller chip. With this interface, the chip can be uniquely configured to work in a variety of applications. On power up, the STORM RFIC is placed in one of two available default states. These power up states make the IC compatible with various baseband ICs.

In order to integrate all of the RF/IF, quantizers and synthesizer into one IC, CONEXANT's 0.35μm silicon BiCMOS process was selected. This process supports inductors with Q's of up to 10, 1fF/μm^2 MIM capacitors and npn transistors with an f_τ of 32GHz. One other feature of this process is that it has usable baluns for single ended to differential conversion. An in depth review of this process can be found in [3].

A. LNA

The schematic for the LNA is shown in Fig. 1. It is a standard cascode amplifier with active bias. The design is very similar to previous work presented in [4]. The reference circuit is biased with a PTAT current to reduce gain variation over temperature. The resistor in the collector is included to lower the Q of the output network, which reduces the gain variation over process and temperature. Since the devices have a very high f_τ, the shunt RC in the output is added to reduce the gain and improve stability at high frequencies. The input is matched with an external series inductor and a shunt capacitor. The LNA has a power gain of 14dB and a NF of 2.0 dB.

B. I/Q Mixer Down Converter

The mixer converts the RF signal from 1.575GHz down to an IF of 1.28MHz. The mixer RF input stage is similar to the LNA circuit with a balun as a load in place of the inductor. The input match for this amplifier is on chip since the NF is not as critical at this point in the receiver chain. The balun at the output of the RF buffer creates a balanced signal to drive an I/Q poly-phase network and the RF input to the mixer. The decision to place the I/Q network in the RF path rather than the LO path was done to reduce power consumption since it had negligible effect on the receiver NF.

The quadrature, differential signals at the output of the poly phase network feed the emitters of the Gilbert cell mixer core. The mixers are followed by a single bipolar differential IF amplifier to preserve the receiver noise figure.

C. VCO

The schematic for the oscillator is shown in Fig. 2. The VCO is a differential LC oscillator with integrated inductors and varactors. The free running VCO phase noise is better than -98dBc @100kHz offset. Low spurious output was a requirement of the oscillator in order to minimize the implementation loss of the receiver. Since power supply ripple can be a major contributor to oscillator spurs, a linear voltage regulator was used on the VCO supply to improve supply rejection.

D. PLL

The architecture of the PLL provides much of the flexibility of this GPS chip. The default mode of operation for the PLL is with the integer-N divide path enabled to the PFD. This is the PLL's lowest power mode of operation. Under the integer-N mode, the PFD can be programmed to accept a divide-by-144 or divide-by-72 output from the VCO, which allows the use of either a 10.949MHz or 21.898MHz reference. For applications that provide an external reference that is not at either of these frequencies, the fractional-N synthesizer is enabled. This is the typical mode of operation for use in a cell phone since a highly stable reference is already available. The PLL fractional-N mode consumes approximately 1.2mA more current than the integer-N mode. A detailed analysis of the fractional-N synthesizer with ΔΣ modulation is described in [5].

E. IF and Quantizers

The IF filter is a 4-pole active Butterworth filter comprised of two cascaded 2-pole stages with unity gain. The design uses two single ended filters for each differential signal and creates a virtual ground between them to improve common mode rejection. There are two selectable bandwidths that are programmable through the three-wire bus. The corner frequencies are 3.5MHz for the narrow band mode and 7MHz for the wide band mode. Stop band rejection is greater than 40dB.

The AGC amplifier consists of 5 cascode differential gain stages. It has 77dB of gain with more than 70dB of dynamic range. Each stage is capacitively coupled and uses a common centroid layout to minimize input offset. The AGC loop is completely internal to the IC.

The quantizer is dual mode. It can perform either 1.5(S>R & S<-R) or 2 bit (Sign & Magnitude) A/D resolutions. The digital outputs are filtered on chip to reduce harmonics, which minimizes potential interference at the L-band input. The quantizer power supply and ground are separate from the rest of the chip to also reduce noise coupling into the receiver.

IV. MEASUREMENTS AND RESULTS

A photo of the Storm IC is shown in Figure 4. The die area for the IC, fabricated in CONEXANT's 0.35um BiCMOS process, is 9mm^2. The IC has separate power supplies for the LNA, Receiver, Quantizers and PLL to reduce power supply noise coupling. Special attention was paid to substrate connections making sure that digital sections did not induce substrate noise into the receiver. The IC is packaged in a 48 pin LGA 7x7mm package.

The total power consumption for the entire chip with the PLL in the integer-N mode and the LNA enabled is 103mW at 2.7V supply. The entire receiver NF is 2.15dB with the LNA and post selector. Fig. 3 shows the out of band interference performance without a pre selector filter in front of the LNA and figure 4 shows the performance with the pre selector in front of the LNA. For both tests there is a post selector filter after the LNA. A summary of the key measured parameters for the Storm IC can be found in Table 1.

V. CONCLUSIONS

A highly integrated, very versatile GPS receiver was presented. The low IF architecture reduces system cost and size while improving out of band interference performance. The multi-mode PLL makes this one of the most highly configurable GPS receivers on the market today. Although targeted for E911 positioning applications, the STORM GPS receiver is a very desirable solution for other portable and hand held navigation applications.

VI. REFERENCES

[1] Young, James P., "A Highly Integrated Commercial GPS Receiver", 2000 IEEE Radio Frequency IC Symposium, pp. 72-78, May 2000.

[2] Dantoni, Holden, Debapriya, "A Highly Integrated GPS receiver for Cellular Handset", 2001 IEEE Radio Frequency IC Symposium, pp. 93-96, May 2001.

[3] Racanelli, M., "BC35: a 0.35 /spl mu/m, 30 GHz production RF BiCMOS technology",
Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting, pp. 125 -128, 1999

[4] Leong, MargaritPregardier, Hull, Magoon, " A 2.7-V 900-MHz/1.9-GHz Dual-Band Transceiver IC for Digital Wirless Communication", IEEE J. of Solid State Circuits, Vol. 34, pp. 286-291 March 1999.

[5] Rhee, Song, Ali, "A 1.1-GHz CMOS Fractional-N Frequency Synthesizer with a 3-b Third-Order ΔΣ Modulator", IEEE J. of Solid State Circuits, Vol. 35, pp. 1453-1460 October 2000.

TABLE 1

Summary of Measured Performance

Parameter	Performance
LNA NF	2.0 dB
LNA Gain	14 dB
RX NF (with LNA and post-select filter)	2.15 dB
Total Power Consumption (Integer-N mode)	103mW @ 2.7V
Total Power Consumption (Fractional-N mode)	106mW @ 2.7V

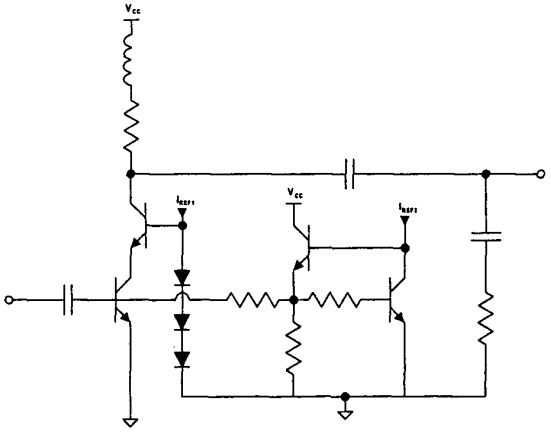

Fig. 1 LNA Schematic

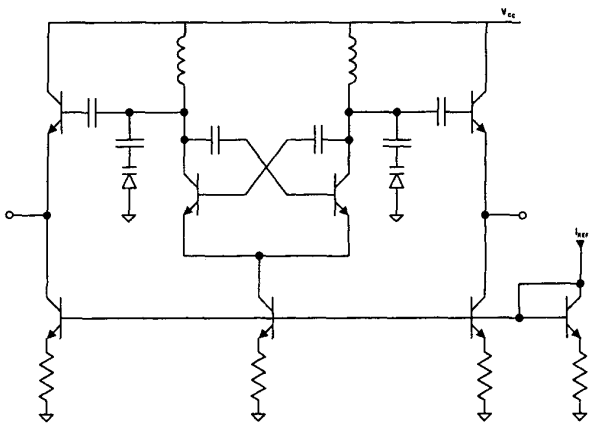

Fig. 2 VCO Schematic

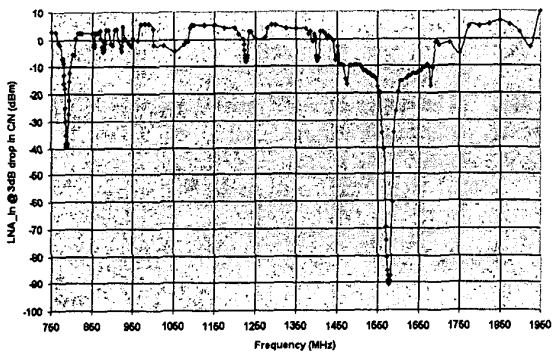

Fig. 3 CW Jamming Level for 3dB drop in C/N (w/o Pre selector)

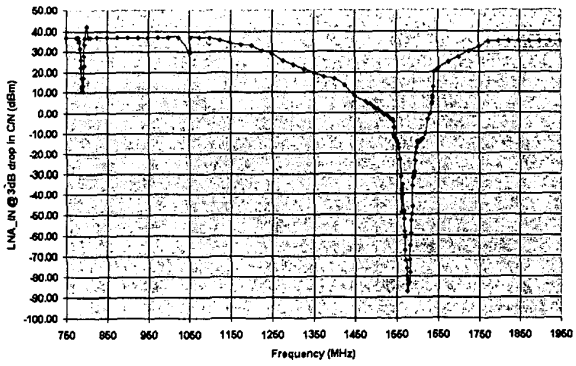

Fig .4 CW Jamming Level for 3dB drop in C/N (with Pre selector)

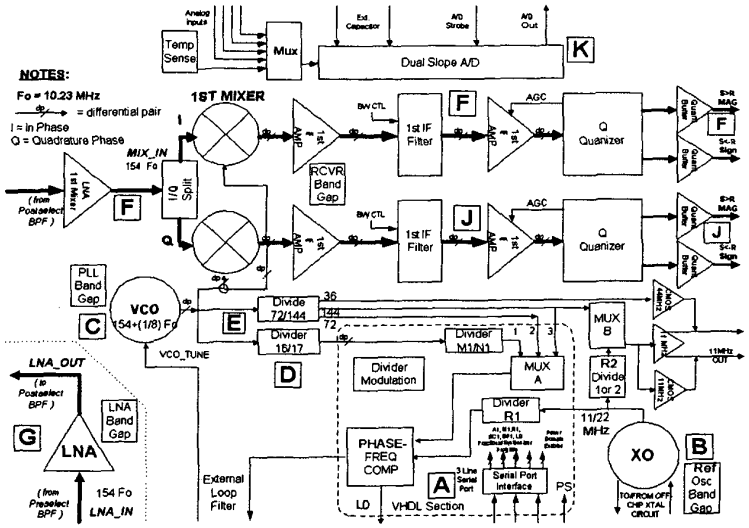

Fig. 5 Storm Block Diagram

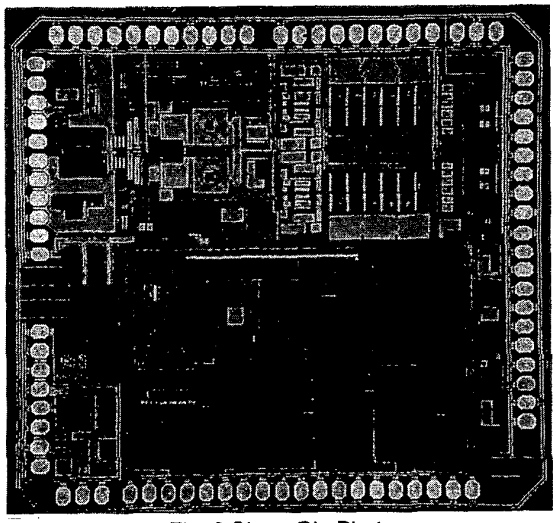

Fig. 6 Storm Die Photo